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10/573,053	03/22/2006	Kim Rishoj Pedersen	GRP-0154	8963

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,053	PEDERSEN ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,16-29,32-34 and 46-53* is/are rejected.

7)☒ Claim(s) *14,15,30,31 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/22/06;5/8/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on 3/22/06. Claims 1 – 53 are pending on this application.

Claim Objections

2. Claim 15 is objected to because of the following informalities: 0dB is not corresponding to high frequencies range of the claimed invention because dB is a unit for power or attenuation while frequency is corresponding to hz.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 6, 8 – 12, 16, 25, 26, 28, 29, 32 – 34, 41, 46, 48, 53 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada U.S. patent No. 6,232,902.

Regarding claim 1, Fig. 2 of Wada discloses A/D converter (12) comprising a self-oscillating modulator (Sigma-delta modulator discloses by Fig. 2 of Wada is a self-oscillating modulator; See Fig. 3 for discloses self oscillating signals of sigma-delta modulator of Fig. 2), said converter (12) comprising at

least one self-oscillating loop (Sigma-delta loop) comprising at least one forward path (forward path of 11, 12, 13), at least one feedback path (feedback path of 14), wherein said at least one forward path (forward path of 11, 12, 13), comprises amplitude quantizing means (12) combined with time quantizing means (13) and outputting at least one time and amplitude quantized signal (D13).

Regarding claim 2, wherein said time quantizing means (13) is arranged within said self-oscillating loop (Sigma-Delta modulator of Fig. 2).

Regarding claim 3, wherein said time quantizing means (13) comprises a high-speed sampling (Col. 2 lines 56 – 57) means (CLK).

Regarding claim 4, wherein said time quantizing means (13) comprises a high-speed one-bit sampler (Col. 14 lines 37 – 39).

Regarding claim 5, wherein said time quantizing means (13) comprises latch-based circuitry (Flip-Flop) comprising at least one latch (Flip-Flop), preferably at least two cascaded latches (prefers only, not limitation).

Regarding claim 6, wherein said amplitude quantizing means (12) and said time quantizing means (13) comprises a multi-bit A/D converter (col. 2 lines 6 – 7) and where said feedback path (14) comprises at least one D/A converter (14) adapted for converting said time quantized signal (D13) into an analogue signal (A14).

Regarding claim 8, Fig. 7 of Wada further discloses wherein said A/D (12) converter comprises two or more self-oscillating loops (2 feedbacks loop of sigma-delta modulator Fig. 7)

Regarding claim 9, wherein said amplitude (12) and time quantizing means (13) comprises an analogue two-level self-oscillating pulse width modulator (See Fig. 3 [D12, D13] disclosing multi-level of pulse-width the sigma-delta modulator of analog to digital converter)

Regarding claim 10, wherein said amplitude (12) and time quantizing means (13) comprises a multi-level self-oscillating pulse width modulator (See Fig. 3 [D12, D13] disclosing multi-level of pulse-width the sigma-delta modulator of analog to digital converter).

Regarding claim 11, wherein said A/D converter (12) is single-ended (single end output of 12).

Regarding claim 12, wherein said A/D converter (12) is differential (differential is inherent to 12 because 12 is comparator, therefore differential must be exist when comparator performing comparing).

Regarding claim 16, wherein said amplitude quantizing means (12) comprises a limiter (11, 15).

Regarding claim 25, wherein said at least one forward path comprises a non-linearity (12, 11).

Regarding claim 26, wherein said non-linearity comprises a limiter (11, 15).

Regarding claim 28, wherein said non-linearity comprises a comparator (12).

Regarding claim 29, wherein said non-linearity comprises an operational amplifier (11).

Regarding claim 32,wherein said at least one forward path (A11, D12) and said at least one feedback path (A14) forms at least one self-oscillating loop.

Regarding claim 33, wherein said self-oscillating loop (Fig. 2) forms a pulse width modulator (Fig. 3 discloses multiples pulse width modulation) and wherein the modulation of an analog input (Ain) signal fed to the at least one forward path (A11, D12) is pulse width modulated (Fig. 3) at least partly by oscillations (oscillation signals of D12, D13) established in said at least one self-oscillating loop (sigma-delta modulator of Fig. 2).

Regarding claim 34, wherein said self-oscillating modulator (Fig. 2) comprises at least one analog input (Ain) connected to said forward path (A!!, D12) and wherein an output (D12) of said forward path is connected to a digital output (D13).

Regarding claim 41, wherein said quantization (13) in a time domain (CLK) is performed within said at least one self-oscillating loop (sigma-delta modulator Fig. 2).

Regarding claim 46, Fig. 2 of Wada discloses a method of pulse width modulating (Fig. 3 discloses a pulse-width modulated output signals D12, D13) an analog input signal (Ain) into a pulse width modulated digital signal, whereby said analog input signal is modulated into a pulse width modulated (Fig. 3 discloses a pulse-width modulated output signals D12, D13) representation by means of at least one self-oscillating loop said self-oscillating loop (sigma-delta modulator of fig. 2) comprising at least one forward path (A11), at least one feedback path (A14), wherein said at least one forward path (A11, A12)

comprises amplitude quantizing means (12) combined with time quantizing means (13) and outputting at least one time and amplitude quantized signal (D13)I.

Regarding claim 48, whereby the method comprises the steps of representing a pulse width modulated (D13, D12) representation as an analogue signal (Ain) and quantizing (13) the pulse width modulation (D12) in the time-domain (CLK) and whereby said pulse width modulated (D12, D13) representation is obtained by means of at least one self-oscillating modulator comprising at least one self-oscillating loop (sigma-delta modulator Fig. 2).

Regarding claim 53, whereby said method is applied in an A/D converter (12) wherein said time quantizing means (13) comprises at least one of an arrangement arranged within said self-oscillating loop (Fig. 2), a high-speed (Col. 2 lines 56 – 57) one bit sample (Col. 14 lines 37 – 39).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7, 13, 39, 42, 43, 44, 47, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada as applied to claims 1 and 46 above, and further in view of Talwalkar et al. U.S. patent No. 7.142,606.

Regarding claims 7, 13, 39, 42, 47, and 52, Wada as applied to claims 1 and 46 above, does not disclose the A/D converter is an audio A/D converter, comprising: decimate filtering means, said filtering means adapted for band pass filtering the time quantized signal , and a down sampling means are connected to said time quantizing means.

Fig. 2 of Talwalkar et al. discloses an audio (Col. 4 lines 39-40) analog-to-digital sigma-delta modulator (213) comprising; decimate filtering means (215), said filtering means adapted for band pass filtering (Col. 5 lines 56 – 57) the quantized signal (208), and a down sampling means (217) are connected to said quantizing means (213).

Wada and Talwalkar et al. are common subject matter for sigma-delta A/D converter. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Talwalkar et al. into Wada for the purpose of eliminate interference of process signal and thus advantageous may facilitate simple processing resources requirement (Talwalkar et al's Col. 11 lines 28 – 32).

Regarding claims 43, Wada/Talwalkar as applied to claim 42 above does not explicitly discloses wherein said decimator (Fig. 2[215] of Talwalkar) comprises having an impulse response which is longer than a period of the pulse width modulated signal (208), preferably at least longer than three times the period of the pulse width modulated signal.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have impulse response of Wada/Talwalkar et al.

to a particular period range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

Regarding claim 44, Wada/Talwalkar does not discloses wherein a stopband attenuation of the underlying antialiasing filter of the decimator (Fig. 2[215] of Talwalkar) is be greater than 60 dB, preferably greater than 100 dB.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to stop band attenuation of Wada/Talwalkar et al. to a particular attenuation range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

7. Claims 17, 19, 20, 21, 23, 27, 35 – 38, 40, 49, 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada as applied to claims 1, 25, and 46 above, and further in view of Gordon et al. Pub. No. 2001/0043153.

Regarding claims 17, 19, 21, 23, 24, 27, and 49, Wada as applied to claims 1, 25 and 46 above, does not explicitly disclose wherein said amplitude quantizing means comprises a frequency compensated limiter; wherein the converter switches with a switch frequency which is at least partly defined by the at least one self oscillating loop; wherein said switch frequency control means comprises an additional periodic signal generator connected to the self oscillating loop; wherein said switch frequency control means comprises an oscillator or a derivative of a clock frequency.

Fig. 6 self-oscillation circuit (Sigma-delta) of Gordon et al. discloses amplitude quantizing means (108) comprises a frequency compensated limiter (106); wherein the converter (108) switches with a switch frequency (lines 6 – 11 of paragraph 0053) which is at least partly defined by the at least one self oscillating loop (94); wherein said switch frequency control means (104) comprises an additional periodic signal generator or a derivative of a clock frequency (period signal at 104 for controlling switching frequency of capacitor 104) connected to the self oscillating loop (94); wherein said switch frequency control means comprises an oscillator or a derivative of a clock frequency

Wada and Gordon et al. are common subject matter for Sigma-delta modulator or self-oscillation circuit. Therefor it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Gordon et al. into Wada for the purpose of providing an improved data acquisition system of the type using delta-sigma converters and having an improved frequency response with nominal spillover (Gordon et al. paragraph 0025).

Regarding claims 20 and 50, Wada/Gordon et al. as applied to claims 19 and 49 above does not explicitly discloses wherein the switch frequency is at least 200 kHz, preferably at least 300 kHz.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have frequency switching of Wada/Gordon et al. to switch at a particular frequency range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the

optimum or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

Regarding claims 35 - 38, Wada as applied to claim 1 above, does not explicitly discloses wherein a transfer functions H(s) is inserted in the forward path, thereby at least partly controlling a switch-frequency; wherein the order of said transfer functions is at least two.

Fig. 6 self-oscillation circuit (Sigma-delta) of Gordon et al. discloses transfer function (106) is insert in the forward path; thereby at least partly controlling a switch frequency (paragraph 0053); wherein the order of said transfer functions is at least two (See Fig. 6 for discloses high orders of transfer function of sigma-delta modulator).

Wada and Gordon et al. are common subject matter for Sigma-delta modulator or self-oscillation circuit. Therefor it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Gordon et al. into Wada for the purpose of providing an improved data acquisition system of the type using delta-sigma converters and having an improved frequency response with nominal spillover (Gordon et al. paragraph 0025).

Regarding claim 40, Wada/Gordon as applied to claims 17, 19, 20, 21, 23, 27, 49, and 50 above discloses every aspect of the claimed invention except for wherein a clock frequency of the time quantizing means is at least 10 (ten) times greater than a switch frequency of said at least one self-oscillating loop, preferably at least 100 (hundred) times greater. It would have been obvious to

one having ordinary skill in the art at the time the invention was made to have clock (Fig. 2 [CLK]) frequency of time quantizer (Fig. 2[13]) of Wada/and switch frequency (Fig. 6[104]) of Gordon et al. at a particular frequency range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

Regarding claim 51, Wada/Gordon as applied to claim 49 above, does not explicitly discloses wherein a clock frequency of the time quantizing means is at least 10 (ten) times greater than the switch frequency of said at least one self-oscillating loop, preferably at least 100 (hundred) times greater. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have clock (Fig. 2 [CLK]) frequency of time quantizer (Fig. 2[13]) of Wada/and switch frequency (Fig. 6[104]) of Gordon et al. at a particular frequency range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada as applied to claim 1 above, and further in view Jensen et al. U.S. patent No. 5,729,230.

Wada as applied to claim 1 above, does not explicitly disclose a variable delay is applied the self-oscillating loop.

Fig. 1 of Jensen et al. discloses a sigma-delta modulator (self-oscillator loop), which a variable delay (26) to.

Wada and Jensen are common subject matter for sigma-delta modulator (self-oscillator). Therefore it would have been obvious to one having ordinary skill in the art a the time the invention was made to incorporate the teaching of Jensen et al. into Wada for the purpose of compensate for processing variations, and dynamically track changes in the signal spectrum's carrier frequency while maintaining a high quality factor, a wide tuning bandwidth, a stable common mode operating point, and a high SNR (Col. 3 lines 19 – 22 of Bair).

9. 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada/Gordon .as applied to claim 21 above, further in view of Chung et al. U.S. patent No. 6,950,488

Wada/Gordon .as applied to claim 21 above does not wherein said switch frequency control means comprises a variable delay.

Fig. 4 Chung et al. Discloses switch frequency control means (440) comprising variable delay (401-408).

Wada/Gordon et al. And Chung et al. are common subject matter for frequency switching. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chung into Wada/Gordon et al. for the purpose of providing: reducing the load of a variable delay unit at high frequency operation and stably synchronization of clocking (Chung; Col. 1 line 19 – 21).

Allowable Subject Matter

10. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach wherein an error originating from at least one time quantizer included in the at least one self-oscillating loop of the converter is suppressed by an error transfer functions which, at low frequencies approximates an inverse of an open-loop transfer functions of said at least one self-oscillating loop.

Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach wherein phase contribution of hysteresis in the non-linearity of the self-oscillating loop is less than 90.degree., preferably less than 40.degree. at a switch frequency.

Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not teach wherein phase contribution of hysteresis in the non-linearity of the self-oscillating loop at switch frequency is less than 20.degree., preferably less than 10.degree.

Claim 45 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims. Prior art does not teach wherein the stopband of the antialiasing filter is: Stopband = kfsout.+/-.BW, where k=1,2,3, . . . until the Nyquist frequency is reached, fsout is the output rate of the decimator and BW is the utility bandwidth, typically preferably at least 20 kHz.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

LINH NGUYEN
PRIMARY EXAMINER

5/21/07

Linh Van Nguyen

Art Unit 2819